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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/598,583	09/05/2006	Adrianus Josephus Bink	NL040236	7385
24737 7590 06/02/2008 PHILIPS INTELLECTUAL PROPERTY & STANDARDS P.O. BOX 3001 BRIARCLIFF MANOR, NY 10510				
EXAMINER				
PETRANEK, JACOB ANDREW				
ART UNIT		PAPER NUMBER		
2183				
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06/02/2008		PAPER		

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

### Office Action Summary

**Application No.**

10/598,583

**Applicant(s)**

BINK ET AL.

**Examiner**

JACOB PETRANEK

**Art Unit**

2183

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 05 September 2006.  
2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.  
3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-20 is/are pending in the application.  
4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.  
5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.  
6) ☒ Claim(s) 1-20 is/are rejected.  
7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.  
8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☒ The specification is objected to by the Examiner.  
10) ☒ The drawing(s) filed on 05 September 2006 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).  
11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a) ☒ All b) ☐ Some \* c) ☐ None of:  
1. ☒ Certified copies of the priority documents have been received.  
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)  
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)  
3) ☐ Information Disclosure Statement(s) (PTO-8508)  
Paper No(s)/Mail Date \_\_\_\_\_  
4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date \_\_\_\_\_  
5) ☐ Notice of Informal Patent Application  
6) ☐ Other: \_\_\_\_\_

#### **DETAILED ACTION**

1. Claims 1-20 are pending.
2. The office acknowledges the following papers:  
Patent Application filed on 9/5/2006.

#### ***Priority***

3. The effective filing date for the subject matter defined in the pending claims in this application is 3/10/2004.

#### ***Drawings***

4. The Examiner contends that the drawings submitted on 9/5/2006 are acceptable for examination proceedings.

#### ***Specification***

5. The disclosure is objected to because of the following informalities:
6. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. The Applicant's cooperation is requested in correcting any errors of which the Applicant may become aware.
7. The abstract of the disclosure does not commence on a separate sheet in accordance with 37 CFR 1.52(b)(4). A new abstract of the disclosure is required and must be presented on a separate sheet, apart from any other text.

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8. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed. The following title is suggested: Compressing and extending pipeline stages dependent on instructions executed.
9. Appropriate correction is required.

***Claim Rejections - 35 USC § 103***

10. The following is a quotation of 35 U.S.C. §103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

11. Claims 1 and 13 are rejected under 35 U.S.C. §103(a) as being unpatentable over Hennessy et al. ("Computer Organization and Design: The Hardware/Software Interface").
12. As per claim 1:

Hennessy disclosed an electronic circuit adapted to process a plurality of types of instruction, the electronic circuit comprising:

first and second pipeline stages (Hennessy: Figure 6.25, pipeline stages MEM and WB); and

a latch positioned between the pipeline stages (Hennessy: Figure 6.25, MEM/WB pipeline register)(It's obvious to one of ordinary skill in the art that the pipeline register can be implemented as a latch.);

wherein the electronic circuit is adapted to operate in a normal mode when processing a first type of instruction in which the latch is opened and closed in response to an enable signal (Hennessy: Figures 6.32 and 6.33, load instruction)(The MEM/WB pipeline register is opened and closed by the inherent clock signal of the processor not shown, which is the enable signal.), and a reduced mode when processing a second type of instruction in which the latch is held open so that the instruction propagates through the first and second pipeline stages without being stored in the latch (Hennessy: Figure 6.33, sub instruction)(The sub instruction is allowed to pass through the MEM/WB pipeline register when the inherent clock is enabled to open the register to allow the instruction to propagate through without storage.).

wherein the first type of instruction requires processing by the first and second pipeline stages (Hennessy: Figures 6.32 and 6.33, load instruction)(The load instruction requires processing by the MEM and WB stages.) and the second type of instruction requires processing by the second pipeline stage (Hennessy: Figure 6.33, sub instruction)(The subtraction instruction requires processing by the WB stage.).

13. As per claim 13:

Claim 13 essentially recites the same limitations of claim 1. Therefore, claim 13 is rejected for the same reasons as claim 1.

14. Claims 1-20 are rejected under 35 U.S.C. §103(a) as being unpatentable over Hennessy et al. ("Computer Organization and Design: The Hardware/Software Interface"), in view of Colwell et al. (U.S. 5,604,878).

15. As per claim 1:

Hennessy disclosed an electronic circuit adapted to process a plurality of types of instruction, the electronic circuit comprising:

first and second pipeline stages (Hennessy: Figure 6.25, pipeline stages MEM and WB); and

a latch positioned between the pipeline stages (Hennessy: Figure 6.25, MEM/WB pipeline register)(It's obvious to one of ordinary skill in the art that the pipeline register can be implemented as a latch.);

wherein the electronic circuit is adapted to operate in a normal mode when processing a first type of instruction in which the latch is opened and closed in response to an enable signal (Hennessy: Figures 6.32 and 6.33, load instruction)(The MEM/WB pipeline register is opened and closed by the inherent clock signal of the processor not shown, which is the enable signal.), and;

wherein the first type of instruction requires processing by the first and second pipeline stages (Hennessy: Figures 6.32 and 6.33, load instruction)(The load instruction requires processing by the MEM and WB stages.) and the second type of instruction requires processing by the second pipeline stage (Hennessy: Figure 6.33, sub instruction)(The subtraction instruction requires processing by the WB stage.).

Hennessy failed to teach a reduced mode when processing a second type of instruction in which the latch is held open so that the instruction propagates through the first and second pipeline stages without being stored in the latch.

However, Colwell disclosed a reduced mode when processing a second type of instruction in which the latch is held open so that the instruction propagates through the first and second pipeline stages without being stored in the latch (Colwell: Figure 3 elements 60-62, column 7 lines 55-67 continued to column 8 lines 1-3)(Hennessy: Figure 6.33, sub instruction)(The combination uses elements 61-62 to bypass the MEM/WB pipeline register when a writeback contention will be avoided.).

The advantage of bypassing an extra pipeline stage that isn't needed for instructions is that these instructions will be allowed to retire earlier and result in increased performance when there is no writeback contention (Colwell: Column 2 lines 65-67 continued to column 3 lines 1-9). One of ordinary skill in the art would have been motivated to modify Hennessy to perform the pipeline stage bypassing of Colwell for the advantage above. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to implement the pipeline stage bypassing of Colwell into the processor of Hennessy for the advantage of increasing performance of the processor of Hennessy.

16. As per claim 2:

Hennessy and Colwell disclosed an electronic circuit as claimed in claim 1, further comprising a latch control circuit connected to the latch, the latch control circuit being adapted to control the latch with the enable signal when the electronic circuit is in the normal mode (Hennessy: Figures 6.32 and 6.33, load instruction)(The MEM/WB pipeline register is opened and closed by the inherent clock signal of the processor not shown, which is the enable signal. The clock signal is part of the processor control

unit.), and to hold the latch open when the electronic circuit is in the reduced mode (Colwell: Figure 3 elements 60-62, column 7 lines 55-67 continued to column 8 lines 1-3)(Hennessy: Figure 6.33, sub instruction)(The combination uses elements 61-62 to bypass the MEM/WB pipeline register when a writeback contention will be avoided, which are the control signals to control the pipeline register.).

17. As per claim 3:

Hennessy and Colwell disclosed an electronic circuit as claimed in claim 2, wherein the latch control circuit receives a signal indicating the mode of operation of the electronic circuit (Colwell: Figure 3 elements 60-62, column 7 lines 55-67 continued to column 8 lines 1-3)(The control logic generates a signal that determines the mode of the processor when Hennessy is acting as a 4 or 5 stage pipeline.).

18. As per claim 4:

Hennessy and Colwell disclosed an electronic circuit as claimed in claim 1, wherein the electronic circuit is adapted to process a third type of instruction, wherein the third type of instruction does not require processing by the second pipeline stage (Hennessy: Figures 6.26 and 6.28, pages 466 and 468, store and branch instructions)(Store and branch instructions don't write to the register file, which is the second pipeline stage, as shown by the control signals in figure 6.28.).

19. As per claim 5:

Hennessy and Colwell disclosed an electronic circuit as claimed in 4, wherein the electronic circuit is adapted to operate in the normal mode until an instruction of the



third type is processed (Hennessy: Figures 6.31-6.34)(The processor acts in a normal mode of processing where instructions are processing in 5 stages.).

20. As per claim 6:

Hennessy and Colwell disclosed an electronic circuit as claimed in claim 5, wherein, after the instruction of the third type is processed, the electronic circuit is adapted to operate in the reduced mode if the following instruction is of the second or third type (Hennessy: Figure 6.26, page 466 and 468, store and branch instructions)(Colwell: Figure 3 elements 60-62, column 7 lines 55-67 continued to column 8 lines 1-3)(When a store instruction is processed, it doesn't write to the register file in the fifth stage, which allows a preceding instruction to write to the register file in the fourth pipeline stage by utilizing the bypass of Colwell. This results in changing the processor to a reducing mode. It's inherent that the bypass can not be utilized if the preceding instruction is a load instruction that must write to the register file in the fifth pipeline stage in the pipelined processor of Hennessy that issued a single instruction per cycle and has a single writeback port on the register file.).

21. As per claim 7:

Hennessy and Colwell disclosed an electronic circuit as claimed in claim 4, wherein the electronic circuit is adapted to operate in the reduced mode until an instruction of the first type is processed (Hennessy: Figure 6.26, page 466 and 468, store and branch instructions)(Colwell: Figure 3 elements 60-62, column 7 lines 55-67 continued to column 8 lines 1-3)(When a store instruction is processed, it doesn't write to the register file in the fifth stage, which allows a preceding instruction to write to the

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register file in the fourth pipeline stage by utilizing the bypass of Colwell. This results in changing the processor to a reducing mode. It's inherent that the bypass can be utilized until a load instruction is executed, which must write to the register file in the fifth pipeline stage.).

22. As per claim 8:

Hennessy and Colwell disclosed an electronic circuit as claimed in claim 1, wherein the first type of instruction includes a load instruction (Hennessy: Figure 6.26)(The load instruction is the first type of instruction.).

23. As per claim 9:

Hennessy and Colwell disclosed an electronic circuit as claimed in claim 1, wherein the second type of instruction includes an arithmetic computation instruction (Hennessy: Figure 6.26)(The add and sub instructions are the second type of instructions.).

24. As per claim 10:

Hennessy and Colwell disclosed an electronic circuit as claimed in claim 4, wherein the third type of instruction includes compare, store, branch and jump instructions (Hennessy: Figure 6.26)(The store and branch instructions are the third type of instructions. Official notice is given that jump and compare instructions don't write results to the register file. Thus, it's obvious to one of ordinary skill in the art to include jump and compare instructions in the processor of Hennessy as the third type of instructions.).

25. As per claim 11:

Hennessy and Colwell disclosed an electronic circuit as claimed in claim 1, wherein the first pipeline stage comprises a data memory (Hennessy: Figure 6.25, MEM pipeline stage.).

26. As per claim 12:

Hennessy and Colwell disclosed an electronic circuit as claimed in any claim 1, wherein the second pipeline stage comprises a write back stage (Hennessy: Figure 6.25, WB pipeline stage.).

27. As per claim 13:

Claim 13 essentially recites the same limitations of claim 1. Therefore, claim 13 is rejected for the same reasons as claim 1.

28. As per claim 14:

The additional limitation(s) of claim 14 basically recite the additional limitation(s) of claim 4. Therefore, claim 14 is rejected for the same reason(s) as claim 4.

29. As per claim 15:

The additional limitation(s) of claim 15 basically recite the additional limitation(s) of claim 5. Therefore, claim 15 is rejected for the same reason(s) as claim 5.

30. As per claim 16:

The additional limitation(s) of claim 16 basically recite the additional limitation(s) of claim 6. Therefore, claim 16 is rejected for the same reason(s) as claim 6.

31. As per claim 17:

The additional limitation(s) of claim 17 basically recite the additional limitation(s) of claim 7. Therefore, claim 17 is rejected for the same reason(s) as claim 7.

32. As per claim 18:

The additional limitation(s) of claim 18 basically recite the additional limitation(s) of claim 8. Therefore, claim 18 is rejected for the same reason(s) as claim 8.

33. As per claim 19:

The additional limitation(s) of claim 19 basically recite the additional limitation(s) of claim 9. Therefore, claim 19 is rejected for the same reason(s) as claim 9.

34. As per claim 20:

The additional limitation(s) of claim 20 basically recite the additional limitation(s) of claim 10. Therefore, claim 20 is rejected for the same reason(s) as claim 10.

### ***Conclusion***

The following is text cited from 37 CFR 1.111(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Patel (U.S. 5,222,240), taught using a temporary register for load instruction results.

Eickemeyer et al. (U.S. 5,778,208), taught using a flexible pipeline for avoiding load interlock dependencies.

Dye (U.S. 6,412,061), taught a dynamic pipeline with reusable logic elements.

Suzuki et al. (U.S. 6,018,796), taught a processor with a variable number of pipeline stages.

Nakajima (U.S. 5,822,561), taught a processor with a variable number of pipeline stages.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jacob Petranek whose telephone number is 571-272-5988. The examiner can normally be reached on M-F 8:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Eddie P Chan/  
Supervisory Patent Examiner, Art Unit 2183

Jacob Petranek  
Examiner, Art Unit 2183

